CBTU0808

Dual lane PCI Express port multiplexer

Rev. 02 — 6 September 2007 Product data sheet

1. General description

The CBTU0808 is a dual lane port multiplexer designed to provide convenient and reliable path switching for PCI Express signals. It is organized as two PCI Express lanes, each consisting of a Transmit and Receive channel. Each channel has four ports, two (A and B) on the source (or host) side and two (A and B) on the destination (or device) side. Each port provides a pair of signal lines to support PCIe differential signaling.

Using specially designed high-bandwidth and high off-isolation switch elements, source and destination ports can be connected or isolated in three possible configurations: source A and B to destinations A and B respectively; or source A to destination B (remaining ports isolated), or all ports isolated.

The switch elements are controlled by internal control logic to set switch positions in accordance with these three configurations, selectable by CMOS inputs CTRL0 and CTRL1 for lanes 0 and 1 respectively. Within a lane, the switch configuration is always applied identically to both transmit and receive channels.

The CBTU0808 is packaged in a 48-ball, depopulated 9 × 9 grid, 0.5 mm ball pitch, thin profile fine-pitch ball grid array (TFBGA) package, which (while requiring a minimum 5 mm × 5 mm of board space) allows for adequate signal routing and escape using conventional board technology.

2. Features

- 2-lane wide PCI Express port multiplexer
- One transmit and one receive differential channel per lane
- Four ports per channel
- PCI Express signaling compliant
- High bandwidth: > 1 GHz
- Low OFF-feedthrough of < –35 dB at 1.25 GHz
- Low channel crosstalk of < –35 dB at 1.25 GHz
- Designed to match characteristic impedance of PCIe signaling environment
- Single 1.8 V supply operation
- ESD resilience of 8 kV HBM
- Available in 48-ball, 5 mm × 5 mm, 0.5 mm ball pitch TFBGA package, Pb-free/Green

3. Applications

- High-performance computing applications
- Port switching and docking applications

4. Ordering information

Table 1. Ordering information

Type number	Solder process	Package		
		Name	Description	Version
CBTU0808EE/G	Pb-free (SnAgCu solder ball compound)	TFBGA48	plastic thin fine-pitch ball grid array package; 48 balls; body $5 \times 5 \times 0.8$ mm	SOT918-1

5. Functional diagram

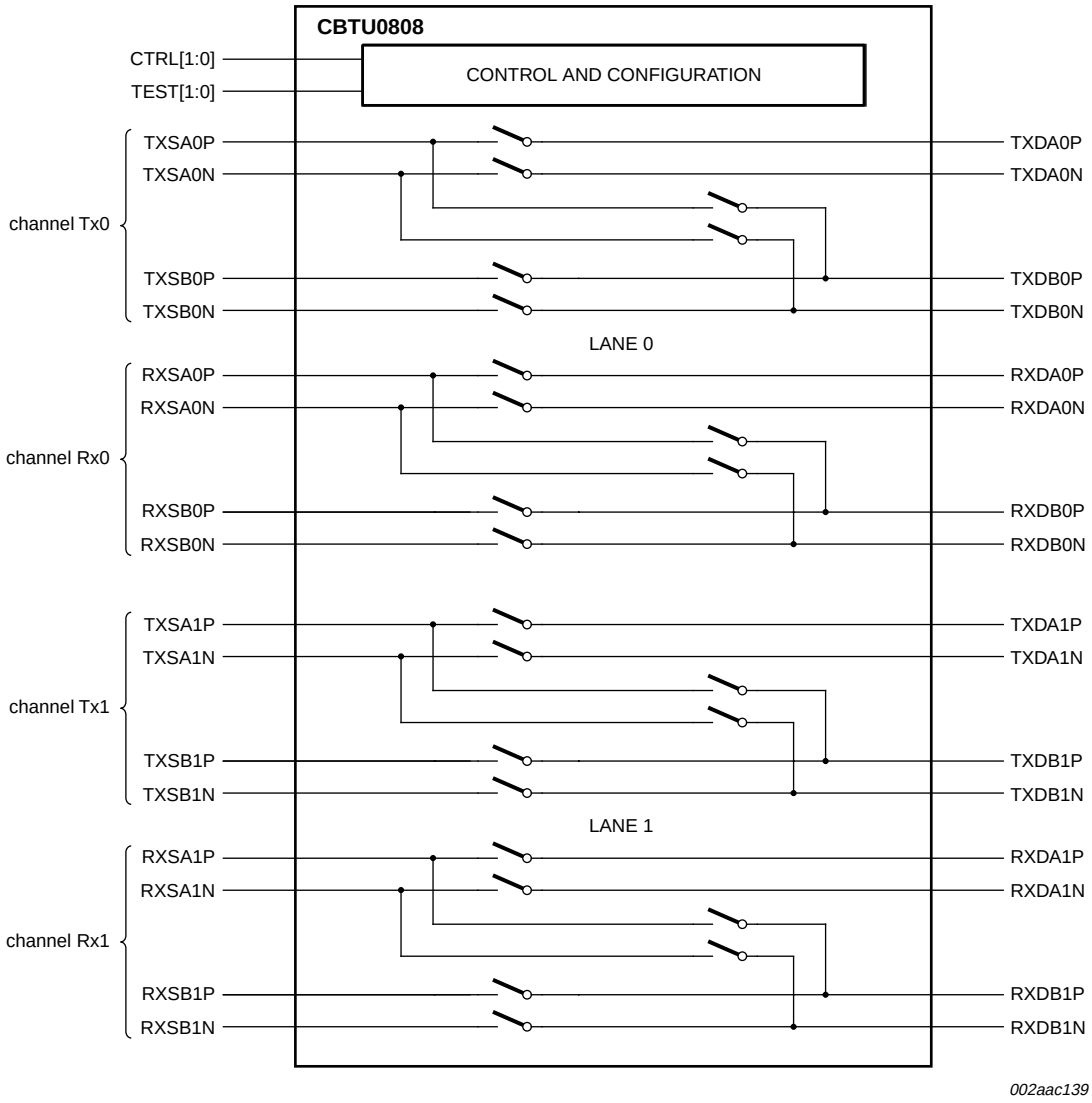
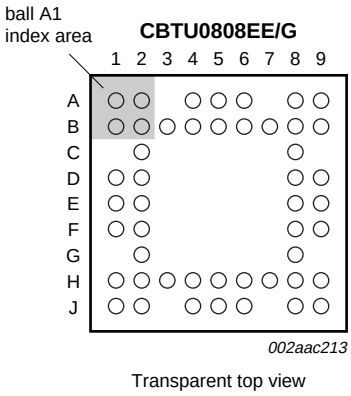


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration for TFBGA48

	1	2	3	4	5	6	7	8	9
A	CTRL0	TXSB0P		TXSA0P	GND	TXDA0P		TXDB0P	TEST1
B	RXSA0P	GND	TXSB0N	TXSA0N	V_{DD}	TXDA0N	TXDB0N	GND	RXDA0P
C		RXSA0N						RXDA0N	
D	RXSB0P	RXSB0N						RXDB0N	RXDB0P
E	GND	V_{DD}						V_{DD}	GND
F	TXSA1P	TXSA1N						TXDA1N	TXDA1P
G		TXSB1N						TXDB1N	
H	TXSB1P	GND	RXSA1N	RXSB1N	V_{DD}	RXDB1N	RXDA1N	GND	TXDB1P
J	TEST0	RXSA1P		RXSB1P	GND	RXDB1P		RXDA1P	CTRL1

002aac212

48-ball, 9 × 9 grid; top view. An empty cell indicates no ball is populated at that grid point.

Fig 3. Ball mapping

6.2 Pin description

Table 2. Pin description

Signal group	Symbol	Pin	Type	Description
Test and control	CTRL0	A1	CMOS input	Switch configuration control inputs. See Table 3 “Switch configuration truth table”.
	CTRL1	J9		
	TEST0	J1	CMOS input	Test input. Used for test purposes only. Should be left open-circuit during normal operation. An internal pull-down resistor will default this pin to a LOW state.
	TEST1	A9	output	Test output. Used for test purposes only. Should be left open-circuit in normal application.
Signal ports	TXSA0P, TXSA0N, TXSB0P, TXSB0N	A4, B4, A2, B3	signal port	Transmit ports A and B differential signal terminals for Lane 0, Source side.
	RXSA0P, RXSA0N, RXSB0P, RXSB0N	B1, C2, D1, D2	signal port	Receive ports A and B differential signal terminals for Lane 0, Source side.
	TXSA1P, TXSA1N, TXSB1P, TXSB1N	F1, F2, H1, G2	signal port	Transmit ports A and B differential signal terminals for Lane 1, Source side.
	RXSA1P, RXSA1N, RXSB1P, RXSB1N	J2, H3, J4, H4	signal port	Receive ports A and B differential signal terminals for Lane 1, Source side.
	TXDA0P, TXDA0N, TXDB0P, TXDB0N	A6, B6, A8, B7	signal port	Transmit ports A and B differential signal terminals for Lane 0, Destination side.
	RXDA0P, RXDA0N, RXDB0P, RXDB0N	B9, C8, D9, D8	signal port	Receive ports A and B differential signal terminals for Lane 0, Destination side.
	TXDA1P, TXDA1N, TXDB1P, TXDB1N	F9, F8, H9, G8	signal port	Transmit ports A and B differential signal terminals for Lane 1, Destination side.
	RXDA1P, RXDA1N, RXDB1P, RXDB1N	J8, H7, J6, H6	signal port	Receive ports A and B differential signal terminals for Lane 1, Destination side.
Power	V_{DD}	B5, E2, E8, H5	power	power supply pins
	GND	A5, B2, B8, E1, E9, H2, H8, J5	power	ground pins

7. Functional description

7.1 Functional description

7.1.1 General information

The CBTU0808 Dual lane PCI Express port multiplexer is designed to allow port switching of up to two PCI Express lanes (each including a Transmit and Receive channel) according to three switch configuration settings (described in Section 7.1.2.1). The basic switch element of the CBTU0808 is designed integrally with its package and chip interconnect to present an optimum characteristic on-impedance when used in a PCI Express signaling environment, and to provide high off-port isolation and low crosstalk.

7.1.2 Functional information

The following paragraphs describe the control and configuration possibilities available in the CBTU0808.

7.1.2.1 Switch configuration

The position of the port switches is controlled by CMOS input signals CTRL[1:0] and can be overridden by CMOS input TEST0 to disconnect (open) all ports between source and destination. For a given lane, the switch positions are always identical between transmit and receive channels. Lane 0 is controlled by CTRL0 and Lane 1 is controlled by CTRL1. The truth table for the switch position as a function of these inputs is shown in Table 3.

Table 3. Switch configuration truth table

Inputs		Function			
CTRLn[1]	**TEST0**	**Source ports[1]**	**Destination ports**		**Comment**
			A	**B**	
LOW	LOW	An	R_{on}	high-Z	SA:DA/SB:DB (Dual Through mode)
		Bn	high-Z	R_{on}	
HIGH[2]	LOW	An	high-Z	R_{on}	SA:DB (Single Cross mode)
		Bn	high-Z	high-Z	
LOW	HIGH	An	high-Z	high-Z	All ports open-circuit (Disconnect mode)
		Bn	high-Z	high-Z	
> LOW	HIGH	Test mode for internal use only			do not use

[1] n is the Lane number (0 or 1).

[2] CTRL1 or CTRL0 = HIGH.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+2.5	V
V_I	input voltage		[1]	–0.5	+2.5	V
I_{IK}	input clamping current	$V_I < 0$ V or $V_I > V_{DD}$		-	–50	mA
I_{OK}	output clamping current	$V_O < 0$ V or $V_O > V_{DD}$		-	±50	mA
I_O	output current	continuous; 0 V < V_O < V_{DD}		-	±50	mA
I_{DDC}	continuous current through each V_{DD} or GND pin			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	Human Body Model; 1.5 kΩ; 100 pF		>8	-	kV
		Machine Model; 0 Ω; 200 pF		>450	-	V

[1] The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage			1.7	-	1.9	V
V_I	input voltage	TXn and RXn ports		–0.25	-	+1.75	V
V_{IH}	HIGH-level input voltage	CTRL[1:0], TEST inputs	[1]	$0.65 \times V_{DD}$	-	V_{DD}	V
V_{IL}	LOW-level input voltage	CTRL[1:0], TEST[1:0] inputs	[1]	-	-	$0.35 \times V_{DD}$	V
V_{ICR}	common mode input voltage range	TXn and RXn ports		0	-	1.5	V
$V_{I(dif)(p-p)}$	peak-to-peak differential input voltage	TXn and RXn ports	[2]	-	-	1.2	V
T_{amb}	ambient temperature	operating in free air		0	-	+85	°C

[1] The CTRL[1:0] inputs of the device must be held at valid levels (not floating) to ensure proper device operation.

[2] $V_{I(dif)(p-p)} = 2 \times |V_{TX\_D+} - V_{TX\_D-}|$. See Paragraph 4.3.3, Table 4-5 of Ref. 1.

10. Static characteristics

Table 6. Static characteristics

Over recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current		[1]	-	-	1	mA
Digital inputs CTRL[1:0] and TEST0							
I_{LI}	input leakage current	$V_I = V_{DD}$ or GND		-	-	±5	µA
C_i	input capacitance	$V_I = V_{DD}$ or GND		-	-	5	pF
Signal ports TXSA0P … RXDB1N							
I_{LI}	input leakage current	$V_I = V_{DD}$ or GND; TEST0 = HIGH (Disconnect mode)		–100	-	+100	µA
$R_{on(sw)}$	switch on-state resistance			8	10	12	Ω
$\Delta R_{on(sw)}$	switch on-state resistance variation	over recommended V_{ID} (input voltage) range		-	0.5	0.75	Ω
$C_{S(ON)}$	ON-state capacitance	V_I = 0.9 V					
		switch; simulated value of the silicon switch only, excluding package parasitics		-	3.6	4.75	pF

[1] Static operating current.

11. Dynamic characteristics

Table 7. Dynamic characteristics

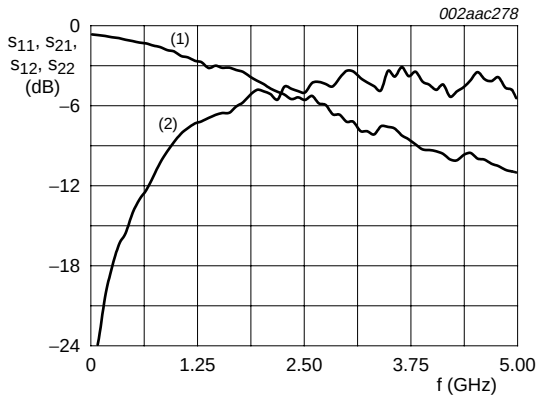
Over recommended operating conditions, unless otherwise noted. Characterization bandwidth: 10 MHz < f_{oper} < 6 GHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PD}	propagation delay	Figure 5	-	60	-	ps
$t_{startup}$	start-up time	supply voltage valid to switch specified operating characteristics	-	-	100	µs
t_{rcfg}	reconfiguration time	CTRL[1:0], TEST0 setting change to switch specified operating characteristics	-	-	100	µs
$t_{sk(o)}$	output skew time	difference in propagation delay between any two 'ON' paths within a channel; Figure 6	-	-	40	ps
$t_{sk(edge)}$	edge skew time	difference of rising edge propagation delay to falling edge propagation delay; Figure 7	-	-	40	ps
$t_{sk(dif)}$	differential skew time	difference in propagation delay between two members of a differential pair; Figure 8	-	-	5	ps
s_{12}	reverse transmission coefficient	Differential mode ON insertion loss; ON-state				
		f = 50 MHz	–0.8	-	-	dB
		f = 625 MHz	–2	-	-	dB
		f ≤ 1.25 GHz	–3.3	-	-	dB
s_{21}	forward transmission coefficient	Differential mode ON insertion loss; ON-state				
		f = 50 MHz	–0.8	-	-	dB
		f = 625 MHz	–2	-	-	dB
		f ≤ 1.25 GHz	–3.3	-	-	dB
s_{11}	input reflection coefficient	Differential mode ON return loss; ON-state				
		f = 50 MHz	-	-	–20	dB
		f = 625 MHz	-	-	–8	dB
		f ≤ 1.25 GHz	-	-	–6.0	dB
s_{22}	output reflection coefficient	Differential mode ON return loss; ON-state				
		f = 50 MHz	-	-	–20	dB
		f = 625 MHz	-	-	–8	dB
		f ≤ 1.25 GHz	-	-	–6.0	dB
s_{12}	reverse transmission coefficient	Differential mode port-to-port crosstalk; ON/OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB
s_{21}	forward transmission coefficient	Differential mode port-to-port crosstalk; ON/OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB

Table 7. Dynamic characteristics *…continued*

Over recommended operating conditions, unless otherwise noted. Characterization bandwidth: 10 MHz < f_{oper} < 6 GHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
S_{12}	reverse transmission coefficient	Differential mode off-port feedthrough; OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB
S_{21}	forward transmission coefficient	Differential mode off-port feedthrough; OFF-state				
		f = 50 MHz	-	-	–35	dB
		f = 625 MHz	-	-	–35	dB
		f = 1.25 GHz	-	-	–35	dB



(1) insertion loss

(2) return loss

Fig 4. S parameters

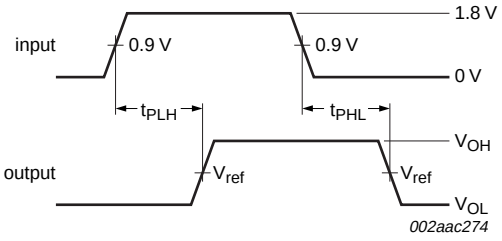


Fig 5. Propagation delay

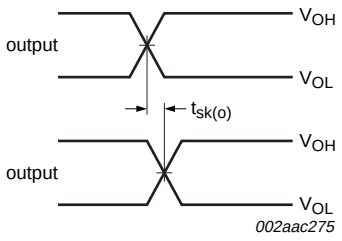
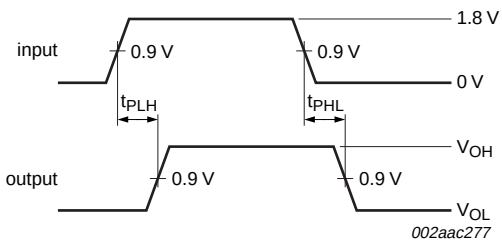


Fig 6. Output skew



$t_{sk(edge)}$ =
$|t_{sk(edge)}$ rising $- t_{sk(edge)}$ falling$|$

Fig 7. Edge skew

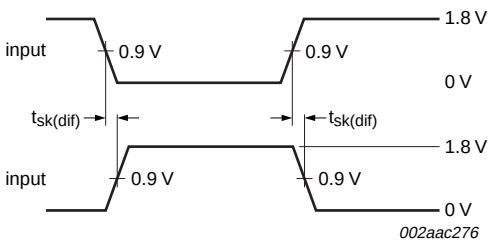
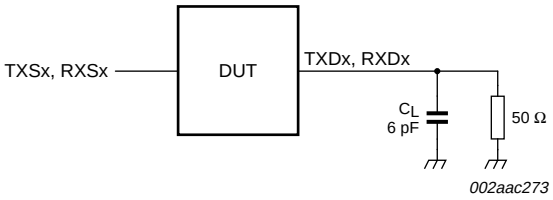


Fig 8. Differential skew

12. Test information



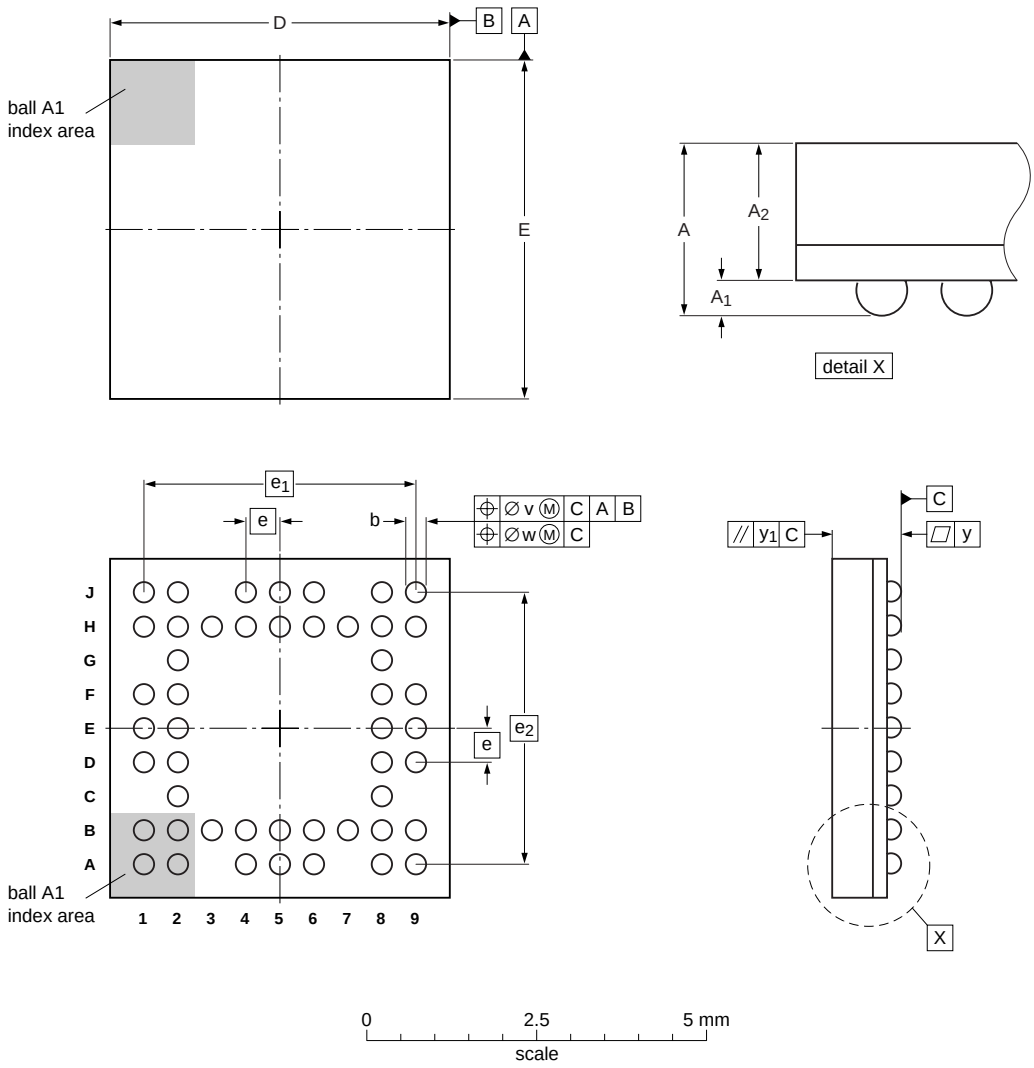
C_L represents board and jig and does not indicate additional capacitance.

All input pulses are supplied by generators having the following characteristics:
PRR ≤ 10 MHz; Z_o = 50 Ω; slew rate = 2.5 V/ns

Fig 9. Test circuit

13. Package outline

TFBGA48: plastic thin fine-pitch ball grid array package; 48 balls; body 5 x 5 x 0.8 mm **SOT918-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.15	0.25 0.15	0.90 0.75	0.35 0.25	5.1 4.9	5.1 4.9	0.5	4	4	0.15	0.05	0.08	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT918-1	- - -	MO-195	- - -			~~05-09-21~~ 05-10-13

Fig 10. Package outline SOT918-1 (TFBGA48)

14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 8 and 9

Table 8. SnPb eutectic process (from J-STD-020C)

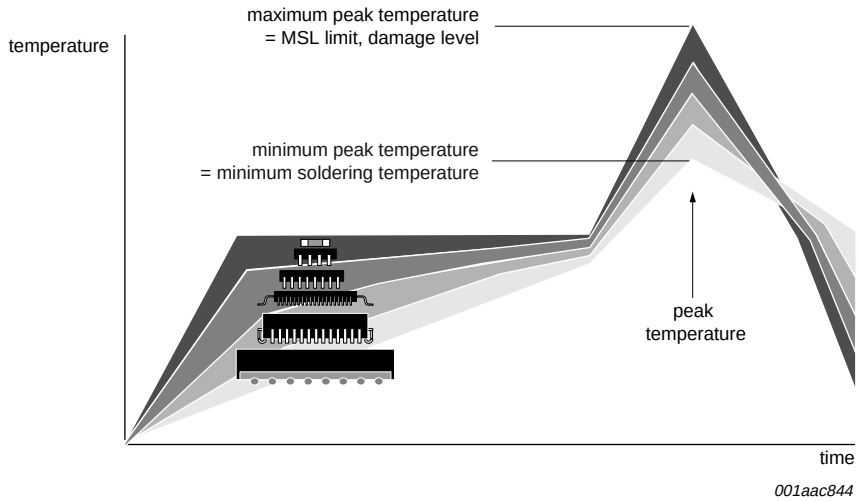
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.



MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
PCI	Peripheral Component Interconnect
PCIe	PCI Express
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Repetition Rate

16. References

[1] PCI Express Base Specification, Rev 1.1 — Revision 1.1, March 2005.

17. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBTU0808_2	20070906	Product data sheet	-	CBTU0808_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 2 “Features”, 10th bullet item: changed “2 kV HBM” to “8 kV HBM” • Table 4 “Limiting values”: changed symbol “I_{CCC}” to “I_{DDC}” • Table 4 “Limiting values”, V_{esd}, electrostatic discharge voltage: – changed minimum Human Body Model from “>2 kV” to “>8 kV” – changed minimum Machine Model from “>200 V” to “>450 V”			
CBTU0808_1	20060602	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contact information

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For sales office addresses, send an email to: **salesaddresses@nxp.com**

20. Contents

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